# Download Hypertransport System Architecture

HyperTransport does not contain dedicated I/O address space. Instead, CPU I/O space is mapped to high memory address range (FD_FC00_0000h— FD_FDFF_FFFFh). Each HyperTransport device is configured at initialization time by the boot ROM configuration software to respond to a range of memory address spaces.HyperTransport is best known as the system bus architecture of modern AMD central processing units (CPUs) and the associated Nvidia nForce motherboard chipsets. HyperTransport has also been used by IBM and Apple for the Power Mac G5 machines, as well as a number of modern MIPS systems.Furthermore, HyperTransport improves reliability and reduces board design complexity. It is scalable and compatible with legacy PC buses, SNA, and PCI. HyperTransport™ System Architecture provides a comprehensive, technical guide to HyperTransport technology. It opens with an overview of HT systems, highlighting the technology's fundamental principles, basic architecture, and its many advantages.HyperTransport System Architecture provides a comprehensive, technical guide to HyperTransport technology. It opens with an overview of HT systems, highlighting the technology's fundamental principles, its basic architecture, and its many advantages.